Radiation Test Results on COTS and non-COTS Electronic Devices for NASA Johnson Space Center Spaceflight Projects

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Abstract**-- This paper reports the results of recent proton Single Event Effect (SEE) testing on a variety of COTS and non-COTs electronic devices and assemblies tested for the International Space Station (ISS) and other spaceflight programs.**

I. INTRODUCTION

The space environment is a very harsh operating environment and the equipment that NASA JSC flies must perform critical functions reliably. Space radiation can directly affect the operation of electronic devices causing unintentional circuit effects such as functional interrupts, transient effects, loss of data or memory integrity, computer crashes and even permanent loss of function of some devices. Therefore, it is imperative that NASA JSC properly characterize electronic devices before these devices are flown in space.

NASA JSC supports the Orion and International Space Station (ISS) programs and must test electronic devices in a method that will meet the applicable program requirements. Due to the shielding of the vehicles under consideration, Total Ionizing Dose (TID) testing is typically not a consideration.

LEO - ISS is a Low Earth Orbit (LEO) application and is tested using 200MeV protons as documented by Dr. O'Neill [3]. The 200MeV beam has been used for over 15 years with positive results and this method is especially valuable for testing board level assemblies and COTS units are commonly tested using this method.

Deep Space – Multi-Purpose Crew Vehicle (MPCV) or Orion 2 is a deep space mission profile and all hardware used for Orion-2 requires heavy ion characterization. An unmanned test flight is planned for this program that will use a similar test method as LEO. Currently MPCV has been tested using traditional heavy ion techniques as well as a new technique under development, which was previously published at NSREC [2], has also been used successfully to characterize some electronic devices for MPCV.

In 2008 through 2012 the Electronic Design and Manufacturing Branch of the Avionics Division of the JSC Engineering Directorate tested at the Indiana University Cyclotron Facility (IUCF), Texas A&M University Cyclotron (TAMU), Lawrence Berkeley National Laboratory (LNBL), and NASA Space Radiation Laboratory at Brookhaven National Laboratory (NSRL). A wide variety of COTS parts such as FPGAs, memories, wireless routers and processors were tested at board level using the high energy protons at IUCF. Individual piece parts were tested at the heavy ion facilities. This paper describes the test protocols, test methods, and analysis methods used to certify these electronic devices and assemblies for flight. A summary of test results is included with a discussion of some select components.

II. TEST PROTOCOL

A. Proton

The majority of JSC hardware used for Shuttle and ISS is tested using 200MeV protons, at IUCF. The proton beam passes through the device losing less than 10% of the initial energy. While the incident protons themselves usually do not cause direct device upsets, they do collide with the nucleus of atoms inside the target device. This collision can fragment the nucleus and then generate a shower of high-energy secondary particles that can cause direct ionization with surrounding atomic nuclei [3]. It is these secondary particles that cause an electronic device to upset, if enough recoil energy is deposited in the sensitive volume. These reactions are rare,

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with approximately one nuclear collision in every 1 x 10^6 incident protons.

The advantages of proton testing are well known, including the fact that the incident 200MeV protons have long range (about 2.5 inches of solid copper is required to stop the beam) and this negates the need to de-lid many device packages. The testing is done in air and usually at ambient temperatures. The large beam diameter of 6 cm (up to 30 cm) is very useful for testing groups of components at the board level. The proton method works great for densely populated circuit boards or for hardware that cannot be easily disassembled for testing. However, the primary drawback of proton testing is that the effective linear-energy-transfer (LET) of the secondary particles are limited to less than 14 MeV cm2/mg and have a short range [3]. Protons do not fully characterize the device's response to radiation compared to heavy ions with the same effective LET. However, this test approach is invaluable as a first-order "Go/No Go" screen for LEO hardware, especially when the responsible Program Office needs to make a selection decisions on a candidate devices within a short time period.

A minimum test fluence of 1x 10^{10} protons/cm2 has been chosen for candidate hardware operating in Shuttle or ISS orbits. The minimum fluence equates to approximately 600 rads (Si) which is about a ten year exposure for hardware operating inside a pressurized spacecraft. This 600 rad includes a conservative factor of 2X for lot-to-lot part variations, and another factor of 2X for environmental uncertainties [4].

The objective of the proton test protocol are to determine the upset failure modes for the hardware in LEO orbits and to establish an estimated mean-time-between-failure (upset) rate for each SEE effect. Of utmost importance is to screen out the very "soft" devices, especially those susceptible to destructive latch-up at low LET values and those with high SEE rates.

For deep space applications proton testing can be a valuable and inexpensive screen for new technology to determine if the part is very "soft". Hardware for MCPV has taken advantage of the quick "Go/No Go" assessment of candidate devices proton testing can provide for selection of critical hardware. However, for deep space applications, heavy ion characterization is required.

B. Heavy Ion

For the MPCV mission to a Near Earth Object (NEO) or the Moon or Mars, heavy ion testing is a necessity. Testing for the MPCV mission, is focused on determining the SEE and the effects of these SEE on the system performance.

JSC uses traditional methods to perform heavy ion testing and require each part be characterized to saturation or failure including high energy, high LET particles. Traditional methods require delidding of the parts, single piece part testing, characterization of the part and application of the part SEE signatures into the system to determine the effects and to apply mitigations. Special attention is paid to Single Event Transients (SET) and the propagation of those transients through the system. Sophisticated data collection systems are required to properly capture the transient signatures.

Testing complex parts and applying those results to complex systems is a difficult task. JSC has been using Radiation Assessment Matrices (RAMs) to evaluate the system level effects while cataloging the effects of each part in the system.

Testing for MPCV has been on-going using Texas A&M University Cyclotron, Lawrence Berkeley National Laboratory and for Variable Depth Bragg Peak Heavy Ion testing at NSRL at Brookhaven National Laboratory.

1) Variable Depth Bragg Peak Method

Variable Depth Bragg Peak (VDBP) Heavy Ion radiation testing differs from traditional heavy ion testing since the electronic components do not have to be delidded in order to be tested. This method also allows more than one electronic part to be tested at the same time similarly to how boards are tested using proton testing. The general methodology of VDBP is that the sensitive volume of the device is not known and that the maximum error cross section occurs at the Bragg Peak LET (Si) value. NSRL has a degrader system setup made of various polyethylene thicknesses which "steps" the Bragg Peak into the sensitive volume of the part to develop the Error Cross Section vs. LET. [5]

III. EXPERIMENTAL METHODS

The goal of each test is to fully exercise the electronic device(s) in the beam while monitoring the appropriate outputs to determine (i) if and when anomalies occur; (ii) what type of error/failure modes they produce; and (iii) what action is needed if any to recover normal operation. The electronic device must be subjected to the proper environment while being operated as close as possible to the flight configuration of the hardware mission.

A. Pretest Preparation – Proton Testing

An initial meeting is held with the project to understand the hardware and its application, as well as specific radiation success criteria. The hardware criticality, mission duration, and any mitigation methods are taken into account when planning the radiation test. A parts list of the hardware is generated and a sequence of beam positions or target areas is mapped out for the candidate hardware. The general project information, parts lists, beam positions and hardware setup and configuration is captured in the project test plans and procedures for documentation.

B. Pretest Preparation – Heavy Ion Testing

Heavy ion testing is requires much more test preparation than proton testing. Electronic parts are required to be delidded and each part must be considered individually. The instrumentation is generally more sophisticated so that Single Event Effects (SEE) such as Single Event Transients (SET) can be catalogued to be used later to determine the system response to the transient signature. Due to the test time for heavy ion facilities, a very detailed test plan is documented, which includes hardware configuration setups, test circuitry, and a recording of exact part numbers and lot date codes as well.

Included in heavy ion testing is the Variable Depth Bragg Peak method. This method is considered for devices in which traditional methods cannot be used. VDBP is especially useful for parts where the sensitive volume cannot be reached due to an epoxy fill or flip chip design parts. [5] The VDBP method can be used for all parts needing deep space testing not just those that are difficult to test by traditional methods.

IV. ANALYSIS METHODS

A. Proton Analysis

Once proton testing is complete, to analyze the data, the errors are grouped by type, frequency and severity. The errors are counted and inputted into a program called PROTEST [6]. PROTEST derives the equivalent 10 year MTBF for the hardware. This software integrates the test data with the LEO radiation environment defined above. It typically assumes worst-case environmental conditions, with 0.1 inch shielding around the device to give a conservative result. The output of PROTEST is the calculated Mean-Time-Between-Failure (MTBF) rate expected for operating the hardware in LEO orbits (expressed in terms of days between failures). An MTBF is calculated for each beam position, as well as a final box-level composite rate. These estimates assume the hardware is operating continuously on-orbit and does not take into account the actual mission timeline in which it will be used. For those devices that show no SEE failures in a typical 1x 10^{10} exposure, we estimate the LEO on-orbit MTBF to be greater than 10 years. This is the same methodology that has been used at JSC since for more than 15 years to evaluate the radiation hardness of mostly COTS hardware with good success.

Even though the SEE events measured were only from proton testing, the MTBF calculated by PROTEST is the composite of both nominal proton (primarily trapped protons in the South Atlantic Anomaly) and the nominal heavy ion (galactic cosmic ray) LEO environments. The proton SEE MTBF is determined using the *Bendel A* method [7]. The heavy ion SEE MTBF derived from proton test data was calculated as described in [3] and [8], using the formula:

$$\mathrm{MTBF}_{HI} = 6 \text{ years / Number of SEE in } 1\text{x } 10^{10} \text{ protons/cm}_2 \quad (1)$$

An alternate method sometimes used to capture the radiation risk, especially for short-duration missions, is the probability of success equation [9]:

$$P_{success} = e_{-(time\ /\ MTBF)} \quad (2)$$

So for a 10-day mission, with a box-level MTBF rate of 1 error every 300 days, the probability of completing the mission without a radiation event is 96.7%. Our test results and MTBF estimates are provided to the project engineering team to determine if the hardware is acceptable to use in their spaceflight application. Results from each test are also entered into a NASA-JSC searchable database for future reference and trending analysis. It should be noted that the MTBF estimates reported are highly dependent on the test configuration and stimulus method used, which again emphasizes the need to test the hardware as close as possible to its intended spaceflight application.

B. Heavy Ion Analysis

JSC uses traditional methods to analyze heavy ion test results. The test data is taken at different LET and ion species until a threshold LET is determined and a saturation cross-sections is achieved. The Weibull curve is determined and the performance in the flight environment is determined as well. The rates are then used to predict the system performance and the individual signatures of each part are documented so that the effect on the overall system due to the part SEE signature is captured.

V. SUMMARY OF DEVICES TESTED

The following section will summarize proton and heavy ion radiation testing on select COTs, Non-COTS hardware and individual electronic parts in a series of summary tables which the JSC Radiation Effects Team has tested over the last 3 to 4 years. Table I gives a list of acronyms commonly used in this paper, and Tables II, III, IV, V will summarize the results of the hardware tested. The results of traditional and the VDBP Heavy Ion testing method will not be shown in the following tables but will be detailed in forward work as testing is ongoing.

TABLE I
LIST OF ACRONYMS

Symbol	Description
CMOS	Complementary Metal Oxide Semiconductor
COTS	Commerical Off the Shelf
DRAM	Dynamic Random Access Memory
DUT	Device Under Test
FPGA	Field Programmable Gate Array
GB	Gigabytes
GHz	Gigahertz
ISS	International Space Station
LDC	Lot Date Code
MB	Megabyte
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTBF	Mean Time Between Failure
N/A	Not Available or Not Applicable
P/N	Part Number
PROC	Processor
SDRAM	Synchronous Dynamic Random Access Memory
SEE	Single Event Effect
SEFI	Single Event Functional Interrupt
SEL	Single Event Latch-up
SET	Single Event Transisent
SEU	Single Event Upset
S/N	Serial Number
TBD	To Be Determined
USB	Universal Serial Bus
UNKN	Unknown

A. Lenovo T61P Laptop Testing

The T61P 15.4" Wide Screen Lenovo Thinkpad Laptop is a commercial off-the-shelf (COTS) device that was tested in 2008. A series of selected hardware which consisted of SDRAMs, Intel Dual Core Processors, and Hard Drives from different vendors and LDCs was tested to determine the best hardware for a final flight laptop configuration. The T61P laptop was an upgrade to the A31P IBM Thinkpad laptops on ISS, which has been in use for the last 10 years on orbit.

The main areas of concern for the laptop were the Processor, Hard Drives, and Memory. Testing of such a complex device requires multiple test dates, repeated testing of various vendors of the same type of hardware, and test result analysis that was used to select the best possible memory, hard drive and processor for the final configuration of the laptop. In preparation for testing, the candidate laptop was completely dissembled down to the motherboard in order to create a detailed parts list of the components of the laptop and to determine the beam positions for testing. Figure 1 shows the beam positions of the laptop on the motherboard. A template of the positions was created on a transparency to affix on the laptop for ease of testing. The major components (processor, SDRAM, hard drive, north and south bridge processors, graphics processor, wireless communication chips and the power chips) of the laptop were isolated in single beam positions to evaluate their potential SEE without multiple active parts being considered as well.

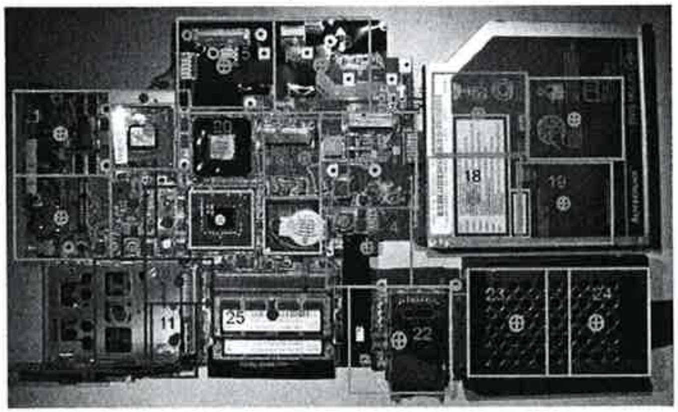

Fig. 1. Beam Position Layout of the Lenovo Laptop (Not shown, beam positions for the laptop LCD screen)

Passmark's Burn In Test software was used to exercise the full capabilities of the laptop and external hardware of the laptop. The software tallied any errors received during testing. The custom software, RWTEST.EXE, was used to test the SDRAM located in the laptop. An $A5 data pattern was written during irradiation then the beam was paused and the SDRAM read for errors. The data pattern was then written during beam off and then read while the proton beam was on. Errors were noted and recorded in the test log during the testing of the SDRAM.

The T61P Laptop was powered using a modified AC adapter cord that was connected to a Sorensen power supply, with the operating parameters set at 16V out and max current at 4.5A. With this modified AC adapter we were able to monitor current to the laptop and voltage at the power supply and going to the laptop. The AC cord was adapted courtesy of the Flight Manufacturing Facility in NASA/JSC EV5 branch.

1) Results of the Lenovo Laptop Testing

Each position was irradiated with a total 600rads (Si) and SEEs were recorded in the data log for each position. For the positions where the hardware could be removed and switched to another vendor supplied component, these positions were retested based on the number of varied vendors for the SDRAM, Hard Drives, and Processors. The results of the test are summarized in Table V. Figure 2 show the laptop in the test cave at IUCF. The radiation testing of the laptop unit and the interchangeable hardware span approximately 18 months and 4 test trips to complete testing and hardware selection for the final configuration of the laptop that would be used in flight.

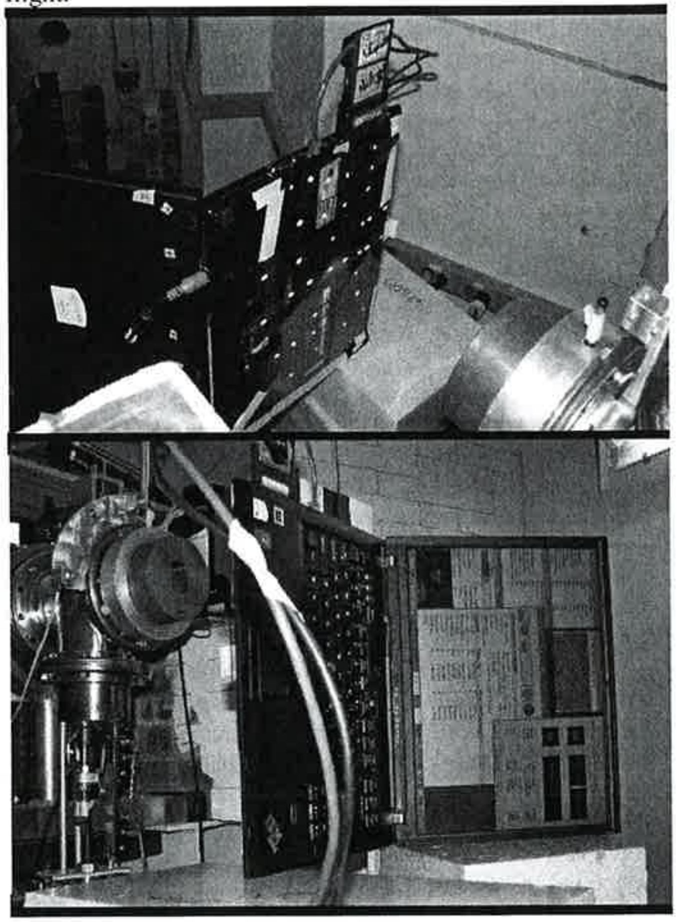

Fig. 2. Lenovo Laptop in IUCF Test Cave

The test report JSC-64085 gives a detailed account of the hardware tested, external hardware accessories, and results of the Lenovo Laptop test and is available on request of JSC Radiation Effects Team.

Table II

SUMMARY OF COTS DEVICES AND ASSEMBLIES FOR LEO APPLICATIONS

Device Category	Space Application	Flight Project	Test Article Description	Device Part Number	Manuf	# Beam Positions Used	Observed Results	Composite MTBF Estimate	Comments
GFE	ISS	Cabin Air Separator for EVA Oxygen	Oxigraft Board, CPU Boards, Digital and Serial I/O Boards	N/A	N/A	35	37 SEFIs in 1.00E10	84 days	
GFE	ISS	Air Quality Monitor	Power Supply and Battery Holder Hardware	N/A	N/A	15	0 Errors in 1.00E10	>10 years	
COTS	ISS	Ammonia Measurement Kit	Drager Chip Measurement Unit		Drager	8	0 Errors in 1.00E10	>10 years	
COTS/ Modifed	ISS	Improved Payload Ethernet Hub and Gateway	Modified Ethernet Hub & Gateway	AN64561	Goodrich	46	32 SEFIs in 1.00E10	57.8 days	
COTS	ISS	ELC Wireless Communications System	COTS Wireless Access Point Bel Air 100n		Bel-Air 100n	19	12 SEFIs in 2.5E10	374 days	Additional dosage was used to evaluate hardware for potential EVA use.
COTS	ISS	Backbone Ethernet Router	48 port Ethernet Switch	MACH4002	Hirschmann	18	27 SEFI in 1.00E10	39.4 days	
COTS	ISS	Power Inverters	120V Power Inverter XP Series	1100 Watt XP Series	ExelTech	16	0 Errors in 1.00E10	>10 years	
COTS	ISS	Power Inverters	28V Power Inverter XP Series	1100 Watt XP Series	ExelTech	16	0 Errors in 1.00E10	>10 years	
COTS	ISS	Oxygen Monitor	Improved Portable Oxygen Monitor	OMT355	Vaisala	23	20 SEFI in 1.00E10	11.8 days	
COTS	ISS	ELC Wireless Communications System	Wireless USB Adapter -	SR71	Ubiquiti	1	0 Errors in 2.5E10	>10 years	Additional dosage was used to evaluate hardware for potential EVA use.
COTS	ISS	Oscillascopes	Portable Oscilloscope and Wave form Generator	MSO-19	Link Instruments	2	3 SEFI +2 SEUs in 1.00E10	359 days	
COTS	ISS	Oscillascopes	Portable Oscilloscope and Wave form Generator	Model #4227	PicoScope	9	7 SEFI + 3 SEUs in 1.00E10	163 days	
COTS	ISS	Hardware Evaluation	Apple iPAD 64GB	MB294LL/A	Apple	9 of 11 tested	9 SEFIs in 1.00E10		The iPAD begin an auto-reboot in Position 9 (iPad Processor) and reverted to factory settings. Retested the Apple Processor and completed the final 3 positions of the total 11.
COTS	ISS	Hardware Evaluation	Apple iPAD 16GB	MB292LL/A	Apple	3	3 SEFIs in 3 positions		
COTS	ISS	GPS Anntena	DC-DC Converter		MDI	1	0 Errors In 1.00E10	>10 Years	
COTS		DVR	FLASH XDR		Convergent Design	10	23 SEFIs in 1.00E10	19.2 days	Did not Function after Test
COTS	ISS	Extravehicular Mobility Unit	USB RS485 Converter	SP390A	Black Box	2	3 SEFI in 1.00E10	895 days	
COTS	ISS	Extravehicular Mobility Unit	Flow Meter	LA-10C	Flocat	2	0 Errors in 1.00E10	>10 Years	

Table III

SUMMARY OF INDIVIDUAL PART TESTING FOR LEO APPLICATIONS

Space Application	Flight Project	Device Category	Part Description	Device Part #	Manufacturer	Composite MTBF Estimate	Observed SEFIs	Comments
ISS	GFE - TEPC	Comm.	Dual 1553 Transceiver	SDG33122172-801	Holt	>10 Years		
ISS	GFE - TEPC	Comm.	GIGABIT ETHERNET PHY	88E1111-B2-BAB-1000	Marvell	1790 Days	1 SEFI in 1.00E10	Manual Reboot
ISS	GFE - TEPC	Converter	DC to DC Converter	SDG33122167-801	Emco	>10 Years		
ISS	GFE - TEPC	Converter	DC TO DC CONVERTER, HIGH RELIABILITY, DUAL OUTPUT ALTERED	SDG33122177-802	International Rectifier	>10 Years		
ISS	GFE - TEPC	Converter	IC, ANALOG TO DIGITAL CONVERTER	MAX188AEAP+	Maxim	>10 Years		
ISS	GFE - TEPC	FPGA	Xilinx Vertex 4 FX Platform FPGA	XC4VFX40-11FFG1152I	Xilinx	157 Days	12 SEFIs in 1.00E10	Manual Reboots
ISS	GFE - TEPC	IC	NPN Bipolar Transistor	MMBT3904LT1G	Fairchild	1790 Days	1 SEFI in 1.00E10	Manual Reboot
ISS	GFE - TEPC	IC	PWM Switcher with Integrated FETS	SDG33122203-801	TI	170 Days	10 SEFIs in 1.00E10	Auto Reboot & Manual Power cycles
ISS	GFE - TEPC	LCD	LCD Display	MTF-TQ35SN741-AV	Mircotips	>10 Years		
ISS	GFE - TEPC	Memory	32MBIT Linear Flash	TE28F320J3D75A	Numonyx	1790 Days	1 SEFI in 1.00E10	Manual Reboot
ISS	GFE - TEPC	Memory	STEC 4GB Compact Flash Card	SLCF4GM1UI	STEC	>10 Years		
ISS	GFE - TEPC	Memory	PLATFORM FLASH, 32-MBIT	XCF32PVOG48C	Xilinx	>10 Years		
ISS	GFE - TEPC	MOSFET	MOSFET, P-Channel Ultra low resistance	SDG33122196-802	International Rectifier	>10 Years		
ISS	GFE - TEPC	MOSFET	MOSFET, N-CHANNEL, PDP SWITCH ALTERED ITEM	SDG33122186-801	International Rectifier	>10 Years		
ISS	GFE - TEPC	MOSFET	P-Channel MOSFET	IRLML6302 TRPBF	International Rectifier	>10 Years		
ISS	GFE - TEPC	MOSFET	MOSFET, Single P-Channel	TPS110D	TI	>10 Years		
ISS	GFE - TEPC	SDRAM	512MB DDR SDRAM	MT4632M16P-5B IT	Micron	516 Days	9 SEFIs in 1.00E10	Manual Reboots

Table IV
SUMMARY OF LENOVO LAPTOP TESTING

Board / Assembly	Part Number	Device Category	Part Description	Manufacturer	Beam Position #	MTBF Estimate	Observed Radiation Events
15.4" Wide LCD Screer	AV3 -#1	LCD Screen	Laptop LCD Screen	Lenovo	Screen 1 thru 12	>10 Years	NONE
15.4" Wide Laptop	AV3 - #1	Power ICs	CPU Power Chips	N/A	1	1790 Days	1SEU + 1F1 in 1E10 F1= Laptop crash req'd. Hard pwr. Cycle to restore. SEU = data verification error
15.4" Wide Laptop	AV3 - #1	Ethernet Ics	Ethernet Chips	N/A	2	>10 Years	1SEU in 1E10 SEU = Error writing to an external HD and creating a file. Req'd. a pwr cycle to clear error.
15.4" Wide Laptop	AV3 - #1	Memory	Graphic Memory	N/A	3	>10 Years	1F1 in 1E10 F1= Laptop crash req'd. Hard pwr. Cycle to restore.
15.4" Wide Laptop	AV3 - #1	Power ICs	Power for SDRAM DIMM	N/A	4	>10 Years	NONE
15.4" Wide Laptop	AV3 - #1	N/A	Docking Staion Connector and Modem Connector Daughter Card	N/A	5	>10 Years	2F1 in 1E10 F1= Laptop crash req'd. Hard pwr. Cycle to restore.
15.4" Wide Laptop	AV3 - #1	N/A	USB Cable Connection	N/A	6	>10 Years	NONE
15.4" Wide Laptop	AV3 - #1	N/A	Additional Ics	N/A	7	1790 Days	NONE
15.4" Wide Laptop	AV3 - #1	Ethernet Ics	Ethernet Chips	N/A	8	1790 Days	NONE
15.4" Wide Laptop	AV3 - #1	Power ICs	1.5V Voltage Regulator	N/A	9	>10 Years	NONE
15.4" Wide Laptop	AV3 - #1	Various	PCMCIA & Other Electronic Chips	N/A	10	>10 Years	NONE
15.4" Wide Laptop	AV3 - #1	Various	PCMCIA & Other Electronic Chips	N/A	11	>10 Years	NONE
15.4" Wide Laptop	AV3 - #1	Various	PCMCIA & Other Electronic Chips	N/A	12	>10 Years	NONE
15.4" Wide Laptop	AV3 - #1	Various	PCMCIA & Other Electronic Chips	N/A	13	596 Days	NONE
15.4" Wide Laptop	AV3 - #1	Core Logic	North Bridge - Mobile Intel GM965 Express Chipset	Intel	14	596 Days	3 SEFI 1 in 1E10 SEFI 1= Laptop crash req'd. Hard pwr. Cycle to restore.
15.4" Wide Laptop	AV3 - #1	Core Logic	South Bridge - Mobile Intel GM965 Express Chipset	Intel	15	357 Days	6F1 in 1E10 F1= Laptop crash req. Hard pwr. Cycle to restore.
15.4" Wide Laptop	AV3 - #1	Optical Drive	DVD RCM - P/N 39T2829 Sept. 2007	Lenovo	16A - 19A	359 Days	3SEU + 1SEFI 1 + 1SEFI 5 in 1E10
15.4" Wide Laptop	AV3 - #1	Optical Drive	DVD RCM - P/N 39T2829 Sept. 2007	Lenovo			SEFI 1= Laptop crash req'd. Hard pwr. Cycle to restore.
15.4" Wide Laptop	AV3 - #1	Optical Drive	DVD RCM - P/N 39T2829 Sept. 2007	Lenovo			SEFI 5 = DVD Read Error
15.4" Wide Laptop	AV3 - #1	Optical Drive	DVD RCM - P/N 39T2829 Sept. 2007	Lenovo			SEU = Error Reading the CD, required a software restart to clear.
15.4" Wide Laptop	AV3 - #1	Optical Drive	DVD RCM - P/N 39T2850 July 2007	Lenovo	16B - 19B	1790 Days	1 SEU in 1E10
15.4" Wide Laptop	AV3 - #1	Optical Drive	DVD RCM - P/N 39T2850 July 2007	Lenovo			SEU = Data error locating files Req'd. a software restart to clear.
15.4" Wide Laptop	AV3 - #1	Optical Drive	DVD RCM - P/N 39T2850 July 2007	Lenovo			
15.4" Wide Laptop	AV3 - #1	Optical Drive	DVD RCM - P/N 39T2850 July 2007	Lenovo			
15.4" Wide Laptop	AV3 - #1	Graphic PROC	Video Graphics Processor	N/A	20	298 Days	5SEFI 1 + 1SEFI 4 in 1E10 SEFI 1 = Laptop Crash required Hard Pwr Cycle to restore. SEFI 4 = Lost of video to on Laptop under test but video feed to control laptop remained.Power cycle to restore.

Table V
SUMMARY OF LENOVO LAPTOP TESTING (CONT)

Board / Assembly	Part Number	Device Category	Part Description	Manufacturer	Beam Position #	MTBF Estimate	Observed Radiation Events
15.4" Wide Laptop	AV3 - #1	PROC	Intel T7700 Dual Core Processor	Inte	21	14.2 Days	11SEFI 1 in 8.83E8 SEFI 1= Laptop crash req'd. Hard pwr. Cycle to restore.
15.4" Wide Laptop	AV3 - #2	PROC	Intel T7300 Dual Core Processor	Inte	21	38 Days	11SEFI 1 in 2.33E9 SEFI 1= Laptop crash req'd. Hard pwr. Cycle to restore.
15.4" Wide Laptop	AV3 - #2	PROC	Intel T7800 Dual Core Processor	Inte	21	26.9 Days	11SEFI 1 in 1.67E9 SEFI 1= Laptop crash req'd. Hard pwr. Cycle to restore.
15.4" Wide Laptop	AV3 - #1	Power Ics	Secure Digital Card Reader and Power Chips		22	>10 Years	NONE
15.4" Wide Laptop	AV3 - #1	Hard Drives	Hard Drive - Hitachi 200GB Full Encryption HD - P/N: 0A53580	Hitachi	23	SEFI=111 Days; SEUs=225 Days	1SEU + 5SEFI 1 in 1E10 SEU = Data Error SEFI 1 = Laptop crash. Req'd hard power cycle to restore
15.4" Wide Laptop	AV3 - #1	Hard Drives	Hard Drive - Hitachi 200GB Full Encryption HD - P/N: 0A53580	Hitachi	24		6SEU + 11SEFI 1 in 1E10 SEU = Data Error SEFI 1 = laptop crash. Req'd hard power cycle to restore.
15.4" Wide Laptop	AV3 - #1	Hard Drives	Hard Drive - Seagate 160GB HD P/N: 98513G-901	Seagate	23	SEFI=74.1 Days; SEU=448 Days	2SEU + 13SEFI 1 in 1E10 SEU = Data Error SEFI 1 = laptop crash Req'd hard power cycle to restore
15.4" Wide Laptop	AV3 - #1	Hard Drives	Hard Drive - Seagate 160GB HD P/N: 98513G-901	Seagate	24		2SEU + 11SEFI 1 in 1E10 SEU = Data Error SEFI 1 = Laptop crash. Req'd hard power cycle to restore
15.4" Wide Laptop	AV3 - #1	SDRAM	SDRAM - Hynix 2GB P/N HYMP325S64AMP8 - Y5 - AB - A 0735 2Rx8 PC2 5300S-555-12	Hynix	25A	223 days	8 bit errors in 1E10
15.4" Wide Laptop	AV3 - #1	SDRAM	SDRAM - Hynix 2GB P/N HYMP325S64AMP8 - Y5 - AB - A 0732 2Rx8 PC2 5300S-555-12	Hynix	25B	63.4 Days	28 bit errors in 1E10
15.4" Wide Laptop	AV3 - #1	SDRAM	SDRAM - Samsung 2GB P/N: M470T5659A20 - CE6 0525 2Rx8 PC2 5300S 555 22	Samsung	25C	52.2 Days	34 bit errors in 1E10
15.4" Wide Laptop	AV3 - #1	SDRAM	SDRAM - Samsung 2GB P/N: M470T5659A20 - CE6 0525 2Rx8 PC2 5300S-555-22	Samsung	25D	BIT Errors =98.7 Days; SEFIs = 895 Days	18 bit errors + 2SEFI 1 in 1E10
14" Standard Laptop	A52 -#1	PROC	Intel T7700 Dual Core Processor	Inte	21	28.5 Days	10 SEFI 1 - 1SEFI 2 in 1.77E9 SEFI 1= Laptop crash req. Hard pwr. Cycle to restore. SEFI 2 = Current to laptop dropped 5A and system froze. Req'd Hard Pwr. Cycle to restore.
14" Standard Laptop	A52 -#1	PROC	Intel T7700 Dual Core Processor	Inte	21	27 Days	11SEFI 1 in 1.63E9 SEFI 1= Laptop crash req. Hard pwr. Cycle to restore.
14" Standard Laptop	A52 -#1	PROC	Intel T7800 Dual Core Processor	Inte	21	35.6 Days	11SEFI 1 in 2.21E9 SEFI 1= Laptop crash req. Hard pwr. Cycle to restore.
14" Standard Laptop	A52 -#1	Core Logic	North Bridge - Mobile Intel GM965 Express Chipset	Inte	14	447 Days	1SEFI 1 + 1SEFI 3 in 1E10 SEFI 1 = Laptop Crash req'd hard pwr. Cycle to restore. SEFI 3 = Lost of ethernet connection req'd power cycle to restore ethernet connection.
14" Standard Laptop	A52 -#1	Core Logic	South Bridge - Mobile Intel GM965 Express Chipset	Inte	15	897 Days	4SEFI 1 in 1E10 SEFI 1 = Laptop crash req'd hard pwr cycle.
14" Standard Laptop	A52 -#1	Graphics PROC	Video Graphics Processor	N/A	20	897 Days	1SEFI 1 + 1SEFI 4 in 1E10 SEFI 1 = Laptop crash req'd power cycle to restore. SEFI 4 = Lost of Video output on the Dut laptop req'd pwr cycle
14" Standard Laptop	A53 - #1	PROC	Intel T7500 Dual Core Processor	Inte	21	25.5 Days	12SEFI 1 in 1.73E9 SEFI 1= Laptop crash req. Hard pwr. Cycle to restore.
14" Standard Laptop	A53 - #2	PROC	Intel T7500 Dual Core Processor	Inte	21	19.6 Days	11SEFI 1 in 1.22E9 SEFI 1= Laptop crash req. Hard pwr. Cycle to restore

VI. CONCLUSIONS

The NASA-JSC Radiation Effects Group frequently tests many commercial microelectronic devices, boards and assemblies for short-term use in LEO applications. The approach we take is a very efficient and cost-effective *"Go/No-Go"* screen for evaluating hardware for payload applications, supplemental avionics, and crew support equipment. Actual on-orbit radiation performance obtained has also been very consistent with our proton-based predictions. Caution must be used in interpreting these results. The data we measured is very dependent on the part's lot-date code, the host board circuit design, DUT setup, and test software used. The duty cycle, input/output signals, and DUT resource utilization are directly related to the device's SEE performance.

As NASA continues to develop plans for returning to the moon and onward to Mars, new radiation-related challenges exist. Mission durations will be longer and the radiation environments are harsher. The avionics used will therefore need to be more reliable, fault-tolerant, and autonomous. The JSC Radiation Effects Team has implemented changes to our current test philosophy and analysis methods required to meet this challenge.

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