MDI's *3646 Mag-Latch Inrush Limiter Application Notes

Model 73646 Programmable Mag-Latch Inrush Limiter Application Notes

The 73646 series are single channel SPST normally open, radiation hardened, positive leg, pulse controlled, current limited inrush limiters using MDI's patented 100K+™ technology. They are intended to control the power input and inrush current to downstream DC-DC converters, which typically have relatively high values of input capacitance. The control input is in the configuration of a mag-latch relay.

The on/off control function is magnetically isolated from the bus voltage. The inrush limiter is normally in the OFF or open mode. It is commanded ON (closed) by a short pulse applied to the LATCH terminals and OFF by a pulse applied to the UNLATCH terminals. In this way, the control function has the same action as a dual coil magnetically latched relay.

This series has four variations for input voltage. Model numbers are prefixed with a 5, 7, 8 or 9 denoting 28, 50, 70 and 100 VDC nominal input variants respectively. They coordinate with all popular satellite bus voltages and harmonize with MDI's comprehensive line of 100K+™Proton Rad Hard DC-DC converters. The information in this application note that references model 73646 applies to all models in the series.

In addition to the magnetically isolated latch/unlatch inputs, the 73646 has two types of inputs referenced to the input bus return: the power bus input, and an inhibit input. Similarly, there are two types of outputs referenced to the input return: the power bus output and the inhibit output. The inputs and outputs are sequenced to first provide controlled initial power application and then inhibit the downstream converters on.

When the inhibit input to the 73646 is un-asserted, the power bus output is inhibited and the inhibit output is un-asserted. When the inhibit input of the 73646 is released, the power bus output turns on, at a limited current. The inhibit output remains un-asserted during the turn on interval until the output power bus is fully saturated at which time it changes state. This function allows the downstream DC-DC converters to be sequenced by the inrush limiter so that the converters are not released from inhibit until their input capacitors are charged and the power bus has reached steady state values. The inhibit is left open (unconnected) if unused; sequencing as above will occur with a Latch command pulse.

Referring to the block diagram, a nominal 15VDC bias voltage is developed relative to the positive input rail.

This bias voltage powers a constant current error amplifier. The input signal for the error amp is derived from a precision shunt on the output of the inrush limiter. The limit is factory set to 4 amperes, but a provision is afforded the user to adjust it via an external

trim resistor. The current gain of the amplifier is largely invariant over line, load, temperature, radiation and life.

An undervoltage lockout is provided so that the output will not start until the lower limit of input voltage is reached. This ensures that the bus is within operating range before downstream converters begin drawing current. A slight hysteresis is built in to prevent chatter.

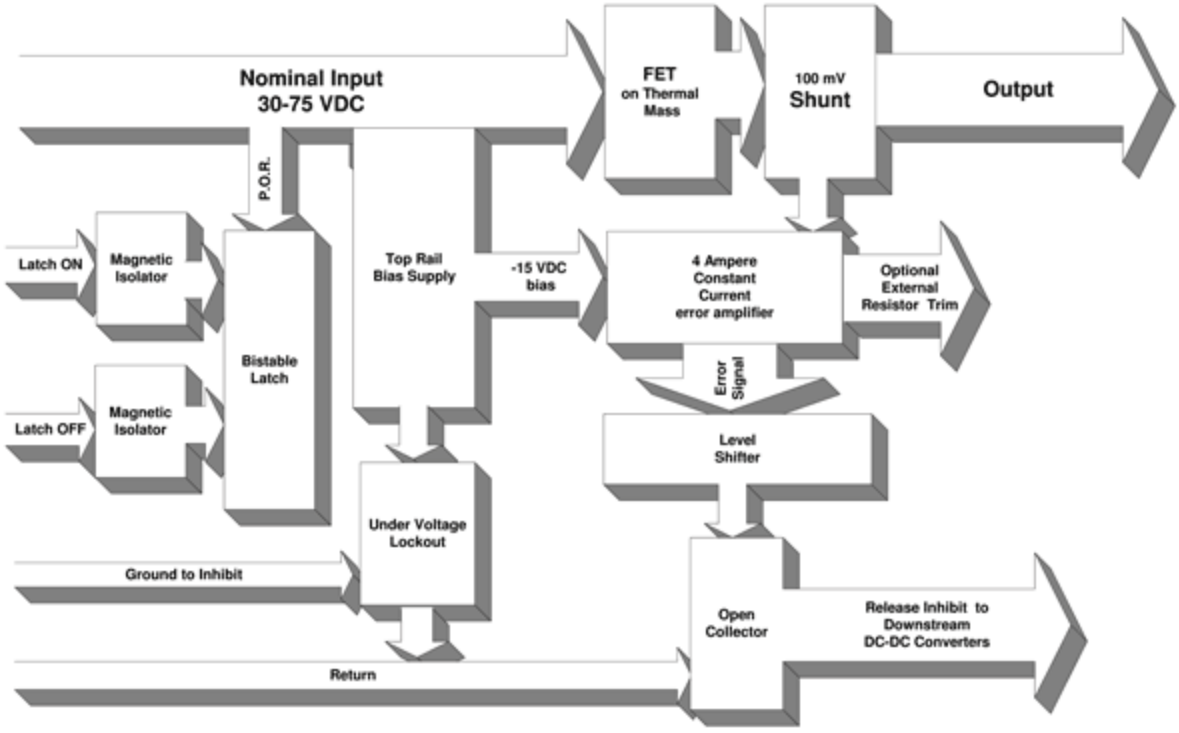
An inhibit interlock is provided for downstream converters so that they remain inhibited OFF until the inrush to their input capacitors is completed. This reduces current surges and minimizes dissipation in the inrush limiter FET, itself fully saturated before downstream converts begin active switching. The error signal of the constant current amplifier is level shifted to ground as the FET achieves saturation, releasing the clamp on the open collector inhibit output transistor.

"Coil" voltage pulses of between 4 and 18 VDC are applied to the Latch ON and Unlatch OFF terminals to command the output and inhibit interlock signal. These ports are magnetically isolated from the input, input return and each other and feed the bistable latching circuit. A failsafe power on reset function always commands the output OFF (Open) with input power removal and reapplication. The "coil" current required is 20 mA typical and a pulse width of 50 mSec is recommended. Activate/deactivate delay is typically 3 mSec.

An important feature of the 73646 inrush limiters is their user selectable output current limit via external resistor. The resistor should be connected between the Rext pin and either power input pin. With the external resistor open, the output current limit is the tabulated value. With a 4K external resistor, the current limit is reduced to 50% of the tabulated value. This feature permits peak output current to be tailored to application requirements and user preference.

Superior stress derating is achieved by close coupling the Inrush Limiter FET to an intrinsic thermal mass. The energy pulse to charge capacitive loads, described as 1/2CV2 divided by the time constant, can create significant thermal dissipation in the FET. Close thermal coupling to the intrinsic mass integrates the temperature rise effects in the FET caused by transient power dissipation.

Simplified Block Diagram



Pin Functions

Pin 1 Latch ON (+)
Pin 2 Latch ON (-)
Pin 3 NC
Pin 4 Unlatch OFF (+)
Pin 5 Unlatch OFF (-)
Pin 6 Case Ground
Pin 7 Inhibit Not (Output)
Pin 8 Inhibit Not (Input)
Pin 9 Inhibit Common Return
Pin 10 Rext (Connect resistor to pin 12
Pin 11 Output +
Pin 12 Input +

Pin Function

Pins 1 and 2 provide Latch ON function to close the switch section. A pulse of between 4 and 18 VDC, 20 mA, 50 mSec. duration is applied, positive to pin 1 and return to pin 2.

Pins 4 and 5 provide Latch OFF function to open the switch section. A pulse of between 4 and 18 VDC, 20 mA, 50 mSec. duration is applied, positive to pin 4 and return to pin 5.

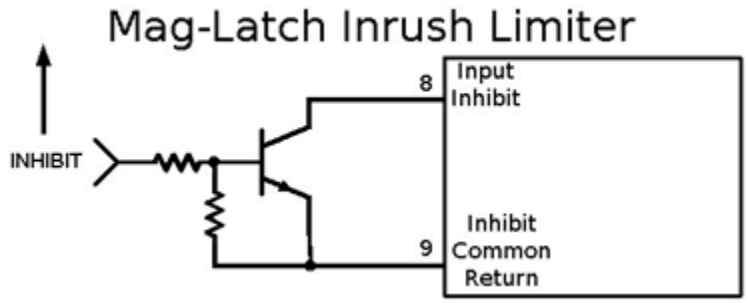
Pin 6 is isolated case.

Pin 7 is the Output Inhibit pin and is connected to the inhibit not inputs of the downstream converter(s). Pin 7 asserts the converters on after the inrush interval is

complete and the power bus has reached steady state range. Up to four MDI converters may be connected and controlled.

Pin 8 is the Input Inhibit pin; pin 9 is the common return.
To inhibit the output voltage, the inhibit input should be connected to the common ground pins, within 0.5 VDC. When the inhibit pin is connected to the common ground, the inhibit current is approximately 100 microamperes.
An open collector transistor may be used to actuate the input inhibit.
Connect pin 9 to input return.
Pin 8 is to be left open (unconnected) if the function is not used.

Input Inhibit Circuit
Preferred Circuit Interface for Input Inhibit



Pins 12 is Input + and 11 is the Output + pin

The FET switch in the 73646 is polarized and the positive input pins should be connected to the positive external circuit point. A body diode is internally connected in the reverse direction. The current rating of the body diode is the same as the switch current rating.

Pin 10 is Rext

Connecting a resistor between pin 10 and pin 12 limits the output current of the inrush limiter. As much as 4K ohms may be added for a 50 percent reduction in tabulated values of output current. This function permits the user to program the current limit and thus, the output rise time into any given capacitive load.

73646 Ratings:

The 73646 mag-latch inrush limiter ratings and characteristics are as described in the table below;

Mag-Latch Inrush Limiter Model	53646 (28 VDC)	73646 (50 VDC)	83646 (70 VDC)	93646 (100 VDC)
Application Bus Voltage	28 VDC	50 VDC	70 VDC	100 VDC
Application Input Voltage Range	18 - 50 VDC	30 - 75 VDC	55 - 90 VDC	80 - 120 VDC
Maximum Recommended Input Voltage	75 VDC	75 VDC	120 VDC	120 VDC
Absolute Maximum Input Range	-0.6 - 100 VDC	-0.6 - 100 VDC	-0.6 - 200 VDC	-0.6 - 200 VDC
Current Limit	4 A	4 A	1.5 A	1.5 A
Undervoltage Lockout	20 V	28 V	55 V	75 V
Initial On Time	250 µSec	250 µSec	350 µSec	500 µSec
Leakage Current at Max Recommended Input Voltage	200 µA	200 µA	20 µA	20 µA
Volt Drop at Rated Current	0.5 V	0.5 V	1 V	1 V
Quiescent Current at Nominal Input	15 mA	15 mA	15 mA	15 mA
"Coil" Voltage	4 - 18 VDC	4 - 18 VDC	4 - 18 VDC	4 - 18 VDC
"Coil" Current	20 mA	20 mA	20 mA	20 mA
Puls Width	50 mSec	50 mSec	50 mSec	50 mSec
Delay to Activate / Deactivate	3 mSec	3 mSec	3 mSec	3 mSec

Power Dissipation:

Total steady state power dissipation of the model 73646 package is limited to 8 watts.

Turn on Time with External Load Capacitance

Turning on into a capacitance causes an inrush current. However, the controlled output current of the model 73646 limits this inrush current. The turn on time will depend on the output load capacitance and the rated output current of the 73646, as adjusted (if any) by the external current program resistor.

Short Circuit and Overload Protection

Model 73646 inrush limiters provide constant current limiting for protection against inadvertent output short circuits and overloads. However, the duration of the short circuit or overload should be limited by thermal constraints.

73646 Heat Removal and Mounting Recommendations

See MDI Application Notes on Recommended Mounting of Hybrids.

Part Numbering System

The model 73646 part numbering system is similar to that used with MDI DC-DC converters. For example:

73646 SE-UF

73646 = Model number for a 50 VDC nominal Inrush Limiter

SE = Grade (available as EU, R, S, RE and SE)

WF = Case Style 8: Seam welded chassis mount package with flange (also available in case styles 2, 3, 5, 6 and 12).

Specifications

- Voltage Drop: *See Table Above*
- I limit max: *See Table Above*
- V input: *See Table Above*
- Leakage current at Voff: *See Table Above*

- Quiescent Bias Current: 15 mA typical
- Inhibit Input Circuit Current: 1 mA typical at 5 VDC
- Control Trip Point: 1.5 VDC nominal
- Inhibit Output: Drives up to 4 MDI DC-DC Converters

- "Coil" Voltage: 4< V< 18
- "Coil" Current: 20 mA typical
- Recommended Pulse width: 50 mS
- Delay to activate/ deactivate: 3 mS typical

- Isolation, All pins to Case: 500 VDC
- Isolation "latch" to "unlatch" coils: 500 VDC
- Isolation "latch" or "unlatch" coils to bus input or return: 500 VDC

- Operating temperature Range: -55°C to 85°C (R or S) or 125°C (RE or SE)
- Storage temperature Range: -65°C to 150°C
- Steady State Power Dissipation: 8 watts

- Total Ionizing Dose: 100K+™
- SEE 82MeV*cm2/mg