73649 Bus Master Application Notes

The 73649 series comprises dual input SPDT normally open, radiation hardened, current limited solid state relay/inrush limiters using MDI's patented 100K$^{+ (TM)}$ technology. These parts enable user selection of redundant satellite buses as well as control the power input and inrush current when series connected ahead of downstream DC-DC converters, which have relatively high values of input capacitance.

This series has four variations for input voltage. Model numbers are prefixed with a 5, 7, 8 or 9 denoting 28, 50, 70 and 100VDC nominal input variants respectively. They coordinate with all popular satellite bus voltages and harmonize with MDI's comprehensive line of 100K+™Proton Rad Hard DC-DC converters. The information in this application note that references model 73649 applies to all models in the series.

The Bus Master hybrid microcircuit is designed to simplify the implementation of redundant power systems in satellite applications. Standard functions include:

- Ability to select power from one or both satellite power buses using a logic level command
- Inrush Current Limiting at turn on
- Ground Referenced Current Telemetry
- Undervoltage Lockout
- Series Redundant FET Switches

The *3649 Bus Master simplifies satellite system electrical design by combining the features of a solid state relay, inrush current limiter and turn-on sequencer to provide: 1) user selection of redundant satellite power buses via logic command; 2) limiting inrush currents to the capacitive inputs of downstream dc-dc converters; and 3) sequencing the active turn-on of those converters via an inhibit signal until their input voltage has achieved steady state value and the inrush interval is complete. Significant reliability gains are thereby achieved.

Operation
The functional block shows two identical constant current inrush limiting power stages. Each power stage, fed from its respective power bus, comprises two series connected FETs close coupled to a thermal mass. The thermal mass integrates the impulse of power dissipation during an inrush current and minimizes the FET's temperature rise.

Solid State Relay – Power Bus Selection
The power section is controlled by independent under voltage lockouts, which prevent the power stage from activating unless a minimum power bus voltage level is present. When either individual power bus voltage exceeds the under voltage minimum, that individual bus may be selected on by grounding the appropriate command pin.

Inrush Current Limiter
The FETs are followed by a current shunt, then connected to the output terminal. Using the shunt resistor signal, the FET drive is the pass stage of a constant current limiter. The un-adjusted constant current is preset to compliment the nominal bus voltage, but may be externally adjusted to a lower value by the user to tailor the output rise time. The output current magnitude, as measured across the shunt resistor, is translated to the input ground level, where it provides a current telemetry signal.

Turn-On Sequencer

In addition to the two identical power circuits, there is a common control circuit. This common circuitry includes a combined inhibit, which can override both bus turn on commands, as well as serves as an inhibit release for downstream DC-DC converters. The inhibit output release allows downstream DC-DC converters to go active only after either of the two bus switches has completed its turn on and inrush limit phase.
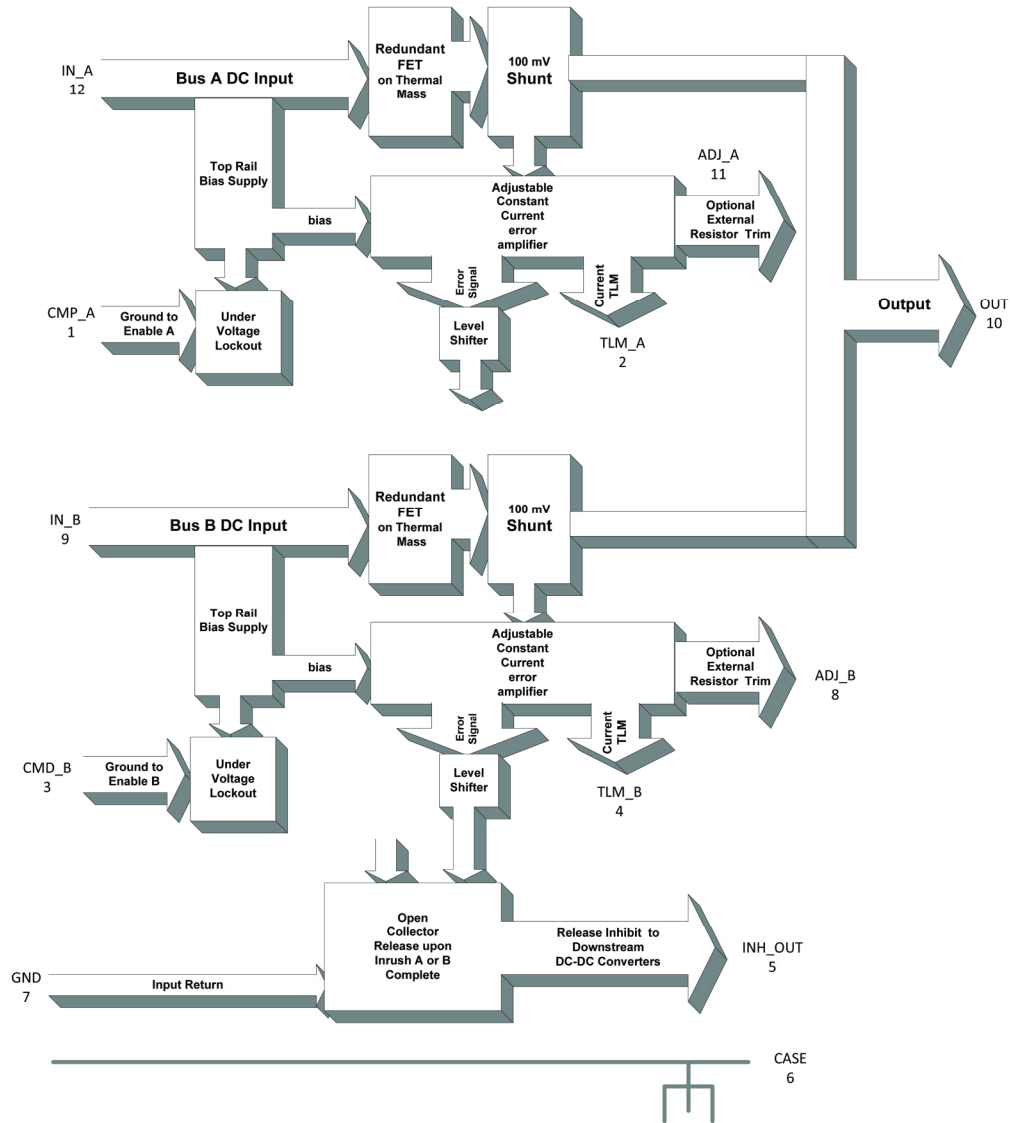
Model Number	Application Bus Voltage	Application Input Voltage Range	Maximum Recommended Input Voltage	Absolute Maximum Input Range	Current Limit	Undervoltage Lockout	Initial On Time	Leakage Current at Max Recommended Input Voltage	Volt Drop at Rated Current	Quiescent Current at Nominal Input	TLM Scaling, Nominal (min-max)	CMD Threshold, Nominal (min-max)
	Vdc	Vdc	Vdc	Vdc	A	V	uSec	uA	V	mA	V/Aout	V
93649	100	80-120	120	-0.6-200	2	75	500	20	1.2	15	2 (1.8-2.2)	2.5 (2.25-2.75)
83649	70	55-90	120	-0.6-200	2	52	350	20	1.1	15	2 (1.8-2.2)	2.5 (2.25-2.75)
73649	50	30-75	75	-0.6-100	4	28	250	200	2.5	14	1 (0.9-1.1)	2.5 (2.25-2.75)
53649	28	18-50	75	-0.6-100	6	17	250	200	2.5	20	0.4 (0.36-0.44)	2.5 (2.25-2.75)

Functional Description

CMD_A, CMD_B

When de-energized, these pins are pulled up to a nominal 10 VDC level. When one pin is grounded, the commanded bus is selected. When both pins are grounded, both buses are connected to the output and to each other. The nominal threshold voltage for actuation is 2.5 VDC and the nominal short circuit current for these pins is 400 microamperes.

TLM_A, TLM_B

A short circuit protected, ground referenced telemetry signal is produced at these pins. The output impedance of the telemetry pins is approximately 1K. The scaling of bus current to open circuit output current is listed in Table 1.

INH_OUT

When the output is in current limit due to limiting an inrush current from either BUS_A or BUS_B (or current drawn from the output in excess of the current limit setting), this pin goes low. In typical applications, the inhibit pins of down stream DC-DC converters in a system are connected to the INH_OUT pin, preventing the downstream DC-DC converters from drawing load current during the inrush limit interval.

This pin is an open collector rated at 80 VDC open circuit and 15 mA short circuit.

ADJ_A, ADJ_B

These pins are used to reduce the constant current limit of power drawn from their respective power buses by adding a resistor from the ADJ pin to its respective power bus. Connecting a 4K resistor from the adjust pin to its adjacent output reduces the nominal current limit by 50%.

BUS_A, BUS_B

These are the power input pins to the device. At least one power bus must be present and above the under voltage lockout limit (listed in Table 1) for the part to function.

Each bus input connects to the output through a pair of back to back FETs, providing failure redundancy.

If both buses are selected, the bus input terminals will be connected to each other through the device.

OUT

The common output pin. The voltage drop from the selected input to the output, at maximum current prior to limit, is shown in Table 1.

*3649 Pin Schedule

Pin Number	Pin Name	Pin Function
1	CMD_A	Ground to enable Bus A
2	TLM_A	Current telemetry output signal – Bus A
3	CMD_B	Ground to enable Bus B
4	TLM_B	Current telemetry output signal – Bus B
5	INH_OUT	Inhibit Output to enable downstream converters
6	CASE	Case connection
7	GND	Input common return
8	ADJ_B	Output current limit adjust for Bus B
9	IN_B	Input + for Bus B
10	OUT	Output
11	ADJ_A	Output current limit adjust for Bus A
12	IN_A	Input + for Bus A

Table 1