5085 POL Application Notes

The 5085 series are radiation hardened, non-isolated, synchronous switching buck point of load (POL) regulators.

Non-isolated DC-DC converters are three terminal devices, having an input terminal, an output terminal and a common terminal.

Buck converters generate an output voltage that is lower than the input voltage,

In simplest form, the buck converter uses a FET, a diode and an inductor.

In order to obtain higher power efficiency, the rectifying diode in the non-isolated DC-DC converter is replaced with a second FET. The forward voltage drop of the diode is usually higher than the drop across the second FET, therefore power losses are lower. The FET must be switched in synchronism with the waveform that would appear across the diode. Therefore, DC-DC converters that use a second FET to perform the action of the diode are called synchronous rectification devices.

Simplified Block Diagram

The block diagram of the model 5085 shows that input power is applied to an upper power switch. The switch is driven at a 100 kHz rate by the pulse width modulator (PWM) circuit.

The switched waveform is then fed through the Buck choke.

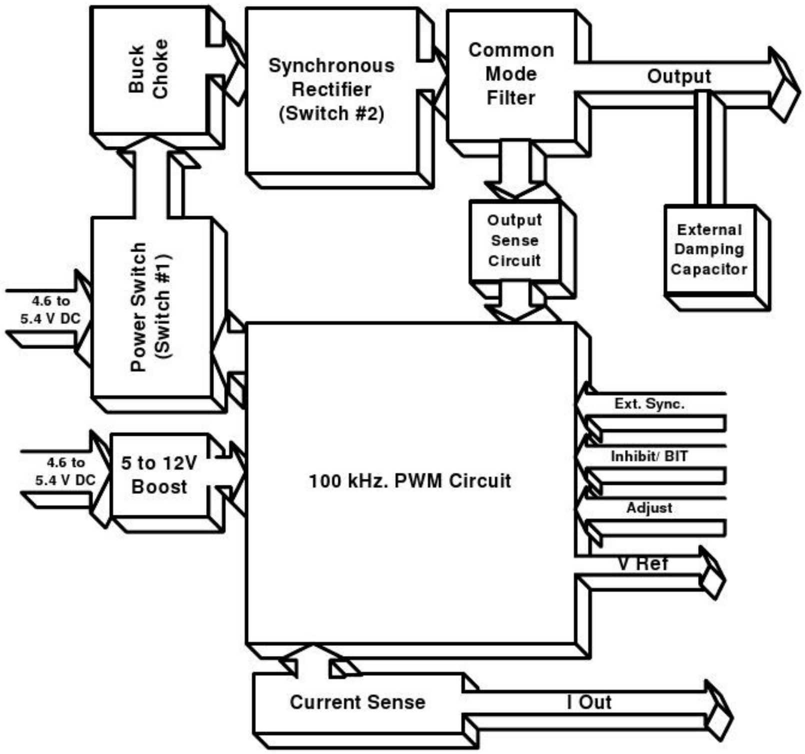
A lower switch is connected in parallel with the output buck rectifier. The lower switch is connected between the upper switch output and ground.

The ripple filtered output passes through a common mode inductor to reduce output spike voltages. The external damping capacitor is supplied by the user to optimize load application and removal transients as well as to lower the output ripple.

The output voltage is passed through the output sense circuit, which permits voltage sensing directly at the 5085's output pins for best static load regulation.

A 5 VDC to 12 VDC boost circuit supplies high level drive signals for the 5085's switching FETs.

Input pins are provided for external sync (this can also be used for phase staggering of multiple 5085's), an inhibit pin and a voltage adjust pin. Output pins include a 5 VDC voltage reference (for output voltage adjustment), a BIT analog output and a current telemetry output (useful in paralleling multiple converters).



Input Voltage Source:

The 5085 converters are intended to operate from a nominal 5 VDC bus and operate over the voltage range of 4.6 to 5.4VDC.

Although the 5085 converters do not contain full internal EMI filters, they do feature common mode filtering on input and output power lines. This provides a substantial reduction of voltage spikes.

A fully loaded 5085 module can draw up to 1500 mA ripple current at its switching frequency of 100 kHz. Therefore, any front end DC-DC converter should provide appropriate decoupling capacitance at it's output terminals to supply this maximum ripple current. A minimum input decoupling capacitance of 30 microfarads (ceramic MLC or low ESR types) per 5085 module is recommended.

Output Voltage:

Output voltage types and adjustment ranges are shown on the 5085 data sheet.

Output Current:

Output current of the 5085 units is limited to 4 amperes or to the current produced at 10 watts output (considering the nominal output voltage), whichever is lower. The maximum output current is constant current limited. For higher output current, consider MDI model 5087.

External Output Capacitance:

Due to the small size of the 5085, the internal output capacitance is limited in value to that necessary for high frequency filtering. For good load transient response, the 5085 data sheet shows a recommended minimum and maximum external capacitance that should be supplied by the user or present in the user's load. The use of low ESR types, such as multiple solid Tantalum chips in parallel is encouraged, as ripple voltage will also be reduced.

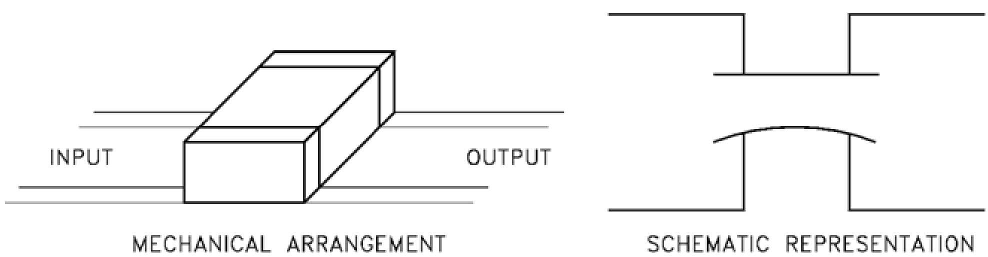
Output Voltage Temperature Coefficients

Voltage limits for Model 5085 parts shown in the MDI data sheets are the nominal 25°C values. At temperatures outside 25°C, the output voltage may vary +/- 100PPM/°C maximum with base temperature.

Output Ripple

Due to its small size, the internal capacitance of the 5085 is limited. For good load removal and load application response, a minimum value of external capacitance is recommended.

When selecting external capacitors, low ESR solid tantalum capacitors are preferred. Capacitor leads with excessive series inductance should not be used, since this will add impedance and negate the benefit of the external capacitance. Relatively large amounts of external capacitance may be added, but do not exceed the data sheet guidelines without consulting MDI.



Four Terminal Capacitor
Method for Improved Filtering

To reduce high frequency spikes, multilayer ceramic capacitors in surface mount chip form can be used. For best results, the capacitor should be connected as a four terminal device (see illustration on previous page). An external series common mode inductor or ferrite beads can also be used between the converter and the capacitor.

Output Ripple Vs. Temperature

The fundamental output ripple of the 5085 converters is primarily dependent on the absolute capacitance value of the external output capacitors (when the output capacitors are multilayer ceramic types), or the ESR of the output capacitors (when the output capacitors are solid tantalum types). The selection of output capacitor depends on the output voltage and type of converter.

However, the following effects occur at temperature. For units using ceramic output capacitors, the capacitance falls off sharply
at high and low temperature extremes. Although the low ESR of ceramic capacitors results in very low ripple voltages, it is not unusual for ripple voltage to double at the high and low temperature extremes. For units using solid tantalum output capacitors, the ESR also rises sharply at low temperature extremes.

Therefore, users should conservatively assume a ripple temperature coefficient of 1% per °C increase over the 25°C base numbers.

Nom.V out	Ext C (min.), uF	Zout (ohms)	Delta V for 50% step	Ext C (max.), uF	Zout (ohms)	Delta V for 50% step
3.3	1000	0.2951	0.4426	4000	0.1119	0.1679
2.5	1000	0.1063	0.2127	4000	0.0557	0.1113
2	1000	0.1063	0.2127	4000	0.0557	0.1113
1.8	1000	0.1063	0.2127	4000	0.0557	0.1113
1.5	1000	0.1063	0.2127	4000	0.0557	0.1113
1.2	1000	0.1063	0.2127	4000	0.0557	0.1113
1	1000	0.1063	0.2127	4000	0.0557	0.1113

Short Circuit and Overload Protection

Model 5085 DC/DC converters contain constant current limiting for protection against inadvertent output short circuits and overloads. The current limiting set point is approximately 125% of rated output current.

Output Over Voltage Protection

Model 5085 DC/DC converters do not contain any internal over voltage protection circuitry. If this function is required, the user should implement it externally. Because the 5085 is non-isolated, in the extremely unlikely event of a failed shorted switching FET, the input voltage could appear at the output pins. If warranted, external OVP should be used.

Output Load Transient response

The output load removal and load application transient voltage is a function of the external capacitance and the magnitude of the current step. The following table lists the magnitude of the output voltage transient for a 25% to 75% rated load change, with the minimum recommended external capacitance.

Back Voltage

A back voltage may be applied to the output of the 5085 DC/DC Converter, whether it be energized or de-energized. Up to 20% above the output voltage rating may be safely applied.

Pin Functions

Pin 1	Positive Input Power Pin
Pin 2	Positive Input Power Pin
Pin 3	Input/Output Common Return
Pin 4	Output
Pin 5	Output
Pin 6	Case Ground
Pin 7	V ref: A nominal +5 VDC reference used for output voltage trimming
Pin 8	Adjust: Input pin used for voltage trimming and paralleling
Pin 9	I out: Signal proportional to output current, for telemetry or paralleling
Pin 10	Sync Input: Input pin used to accept external 100 kHz sync signal
Pin 11	BIT: An analog output line indication the module status
Pin 12	Inhibit-Not (Ground to inhibit)

Voltage Reference (Pin 7)

The voltage reference pin is primarily used for downward voltage adjustment of the output. However, it may also be used for other applications. Up to 10 milliamperes may be drawn by the user. This current, if used, is ultimately drawn from the input voltage.

Output Voltage Adjustment (Pin 8)

The adjust pin function (pin 8) allows the user to set the 5085 output voltage slightly above or below it's initial set point. The recommended adjust range for each part type is listed in the data sheet.

When trimming for an increased output magnitude the adjust resistor is connected to the common ground. When trimming for a decreased output magnitude the adjust resistor is connected to the V ref pin (pin 7).

The adjust pin is connected to an internal 10K resistor, whose purpose is to prevent damage to the internal circuits and to reduce noise pickup.

The following table gives applicable resistor values for each 5085 type, as well as which equations to use to calculate the external adjust resistor value. For purposes of computing the external adjust resistor power dissipation, a maximum of 2.5 VDC appears across the external adjustment resistor.

If the external adjust feature is not used, both the adjust pin (8) and the V ref pin (7) should be left unconnected.

When the converter is adjusted upwards, the output power should be limited to 10 watts, or the output current should be limited to 4 amperes, whichever is less.

Vout	R1	R2	R3	Equation for Upward Adjust	Equation for Downward Adjust
3.3	16K	50K	10K	Equations 1A and 3	Equations 2A and 3
2.5	10K	Infinity	10K	Equations 1A and 3	Equations 2A and 3
2	10K	50K	10K	Equations 1B and 3	Equations 2B and 3
1.8	10K	35.7K	10K	Equations 1B and 3	Equations 2B and 3
1.5	10K	25K	10K	Equations 1B and 3	Equations 2B and 3
1.2	10K	19.23K	10K	Equations 1B and 3	Equations 2B and 3
1	10K	16.67K	10K	Equations 1B and 3	Equations 2B and 3

Equation 1A $$\frac{V_{Adj}-2.5}{R_1}=\frac{2.5}{R_2}+\frac{2.5}{R_4}$$

Equation 1B $$\frac{2.5-V_{Adj}}{R_1}=\frac{2.5}{R_2}-\frac{2.5}{R_4}$$

Equation 2A $$\frac{V_{Adj}-2.5}{R_1}=\frac{2.5}{R_2}+\frac{2.5}{R_4}$$

Equation 2B $$\frac{2.5-V_{Adj}}{R_1}=\frac{2.5}{R_2}+\frac{2.5}{R_4}$$

Equation 3 $$R_3=R_4-10k$$

Output Current (Pin 9)

An analog of the output current is provided in pin 9. This is useful in paralleling applications.

Model 5085 Pin 9 millivolts per output ampere scaling

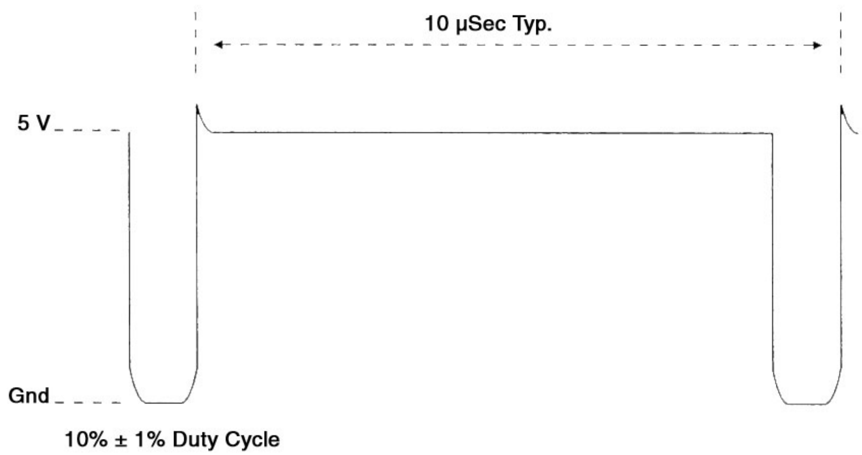
Nom.Vout	Vin=5 VDC
3.3	90
2.5	68
2	55
1.8	49
1.5	41
1.2	32
1	27

Sync Input (Pin 10)

Pin 10 is the Sync Input. The 5085 hybrid operates at approximately 95 kHz and may be synchronized to frequencies from 95 to 105 kHz. The sync input pulse should meet the following levels as shown in the diagram. The sync input should sit at nominal 5 VDC and transition to ground level at a 10% ± 1% duty cycle. It should be noted that the internal oscillator runs at the switching frequency. Other frequencies are also available on special order. Contact MDI's Sales and Marketing Department for other sync frequencies.

Synchronizing the power conversion units within an extremely sensitive system ensures that any noise generation is coincident with the system clock.

If two or more 5085 units are used, a phase staggered sync signal may be applied in order to reduce the overall input and output ripple. The "sync pin" should be left open if unused.



Typical Sync Waveform

Inhibit/BIT (Pin 11,12)

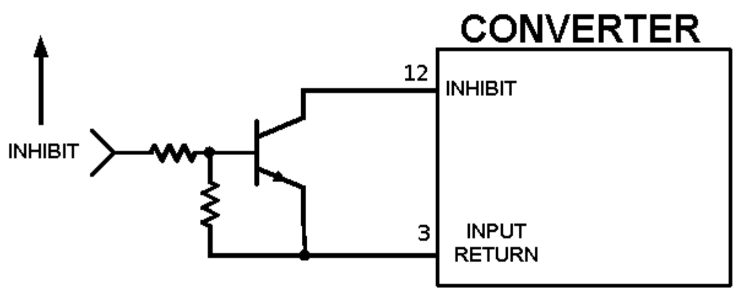
Pins 11 and 12 are the BIT/Inhibit pins.

The BIT signal is an analog signal that is the buffered output of the internal PWM error amplifier. The source impedance of the BIT line is approximately 50K ohms.

The normal voltage range of the BIT line is 0.9 VDC to 3.3 VDC. A voltage lower or higher than these values indicates that the internal regulating loop considers the output voltage to be too high or too low, respectively

The BIT line may be connected to an external comparator window detector to produce a discrete BIT signal.

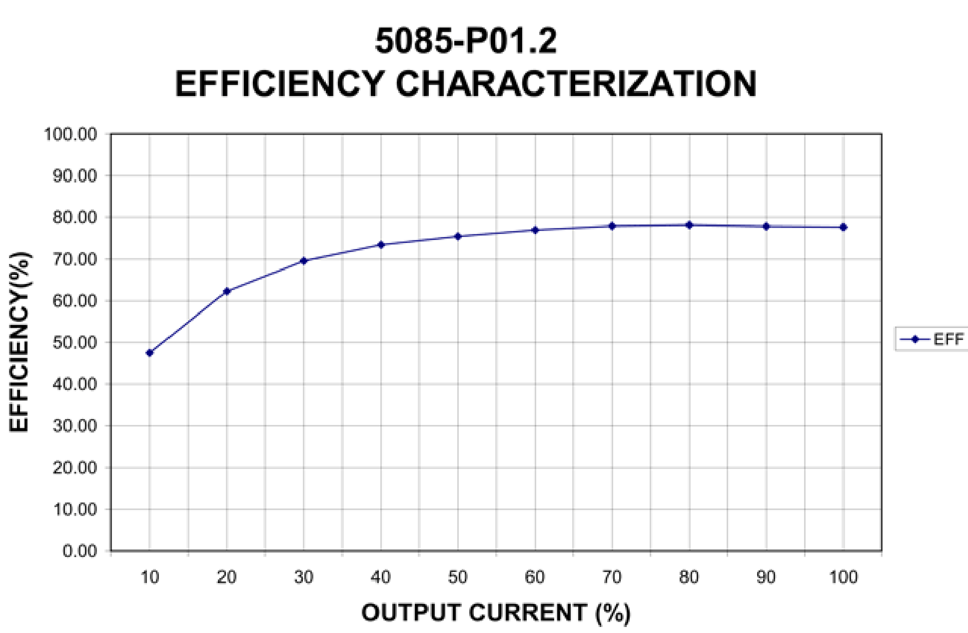
Pin 12 is also the Inhibit pin. To inhibit the output voltage, the inhibit input should be connected to the input/output return (pin 3) to within 0.5Vdc. When so connected, the current through the pin is approximately 100 microamperes. An open collector transistor may be used to actuate the inhibit as shown below.



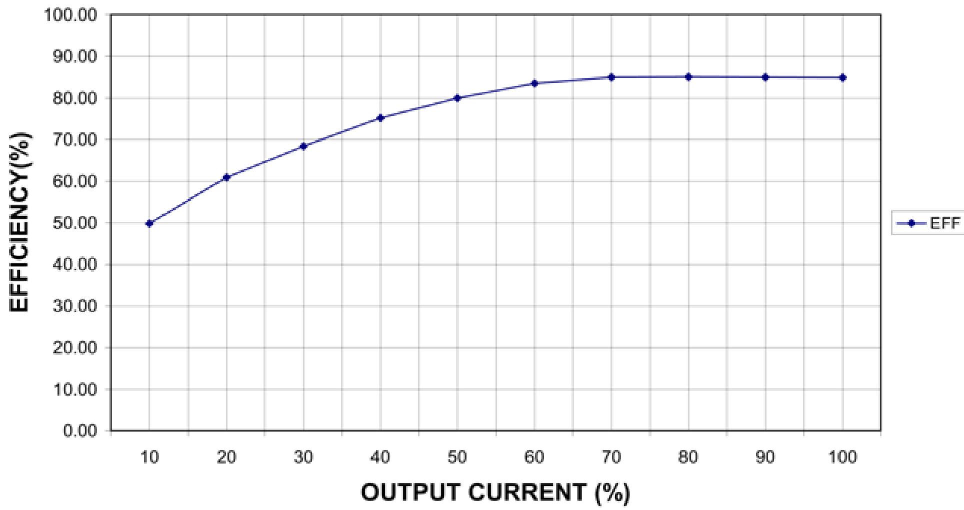
Preferred Circuit Interface for Inhibit

Efficiency of 5085 POL Converters

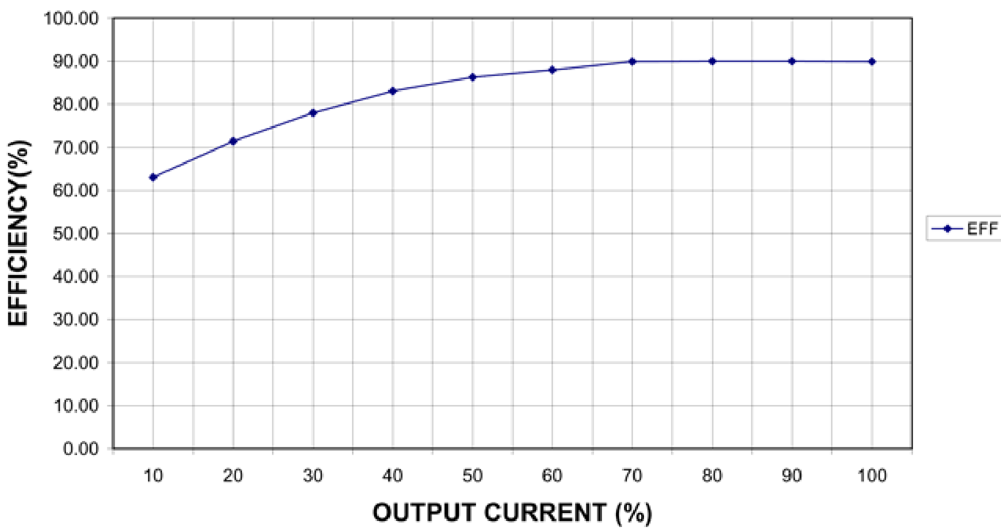
Dual FET synchronous rectification and non-isolated design afford very high operating efficiencies for the 5085 series POL converters. Even very low operating voltages of 1.2Vdc or less achieve typical efficiencies exceeding 78 percent, while models with outputs of 3.3Vdc and higher reach 90 percent or more. The characteristic curves below give graphic representation of typical efficiencies achieved as a function of load at 5Vdc input.



5085-P02.5
EFFICIENCY CHARACTERIZATION



5085-P03.3
EFFICIENCY CHARACTERIZATION



Some advice about protection of sensitive loads

The 5085 POL converters comprise a non-isolated circuit design; there is no inherent galvanic barrier that isolates the input bus from the output side of the converter. Under some circumstances of overstress or failure originating outside the converter, the converter itself may fail short circuit, effectively coupling input to output for some duration. Therefore, the user should assess the application risk to the loads under such conditions and make provisions to implement OVP, zener clamps or voltage suppression components as may be deemed necessary. Please contact the factory for assistance.

5085 Heat Removal and Mounting Recommendations

See MDI application notes on mounting considerations for DC/DC Converters.

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